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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,639	09/18/2003	Hiroki Koga	N34771600WD1	6100

7590

07/26/2005

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EXAMINER
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LE, THAO X

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/665,639

Applicant(s)

KOGA, HIROKI

Examiner

Thao X. Le

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3, 5-7 and 17-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 28 is/are allowed.
- 6) ☒ Claim(s) 1, 3, 5-7 and 17-27 is/are rejected.
- 7) ☒ Claim(s) 20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Allowable Subject Matter***

1. The indicated allowability of claim, 17-20 and 29 are withdrawn in view of the newly discovered reference(s) to Kim (US Pub 2002/0001935). Rejections based on the newly cited reference(s) follow.

### ***Specification***

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: No drawing shows the limitation 'first spacing from the first contact to the first gate electrode is greater than a second spacing from the second contact to the second gate electrode' of claim 20. The fig. 8 (d) seems to indicate the opposite because the SA region would be the first region having first contact 113 and the spacing of the first contact to the first gate electrode 100A seems to be smaller than the spacing of the second contact to the second gate electrode 100B (region SB).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3, 6-7, 17-19, and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub 2002/0132403 to Hung et al in view of US Pub 2002/0001935 to Kim et al.

Regarding claims 1, Hung discloses a semiconductor device in fig. 5 including an insulated gate field effect transistor (IGFET), comprising: a gate electrode of the IGFET having a lower layer electrode 6 [0018] formed on a gate insulating film 4 [0018], and an upper layer electrode 6a [0018], formed on the lower layer electrode 6; a cap film 8 [0019], formed on the upper layer electrode 6a, a first nitride film 12 [0002] on a side surface of the upper layer electrode 6a; an oxide film 10 [0018] on a side surface of the lower layer electrode 6; and an etching stopper film including a second nitride film 20 [0021] formed on the outside of the first nitride film 12 and an outside of the oxide film 10, wherein the first nitride film has a film thickness of about 5 nm [0020].

But Hung does not disclose the first nitride film does not cover the side surface of the cap film.

However, Kim discloses a semiconductor device in fig. 2H including a lower gate electrode 22a disposed on a gate-insulating layer 21, and an upper gate electrode 29 disposed on the lower gate electrode 22a, an oxide film 24 on the side surface of the lower electrode 22a and a nitride film 25 on a side surface of the upper gate electrode 29, fig. 2H. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the nitride film 25 teaching of Kim with Hung's device, because it would have prevented transformation of the gate electrode as taught by Kim, see abstract.

Regarding claims 2-3, 6-7, and 22-24 the process limitations "thermal nitride film" in claim 2, "rapidly heated thermal nitride" in claim 3, "thermal oxide film" in claims 6, 23, and "nitride film is formed with CVD" in claims 7, 24 do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 17, Hung discloses a semiconductor device including a first region and a second region in fig. 5 comprising: a first gate electrode 6 of a first IGFET in the first region (right side) having a first lower layer electrode 6 formed on a first gate insulating film 4 and a first upper layer electrode 6a formed on the first lower layer electrode 6; a first cap film 8 formed on the first upper layer electrode 6a; a first nitride film 12 on a side surface of the first upper layer electrode 6a; a first oxide film 10 on a side surface of the first lower layer electrode 6; a first etch stop film including a second nitride film 20 formed on the outside of the first nitride film 12 and first oxide film 10, fig. 5; a second gate electrode 6 of a first IGFET in the first region (left side) having a second lower layer electrode 6 formed on a second gate insulating film 4 and a second upper layer electrode 6a formed on the second lower layer electrode 6; a second cap film 8 formed on the second upper layer electrode 6a; a third nitride film 12 on a side surface of the second upper layer electrode 6a; a second oxide film 10 on a side surface of the second lower layer electrode 6; a second etch stop film including a second nitride film 20 formed on the outside of the second nitride film 12 and second oxide film 10, fig. 5; wherein the first IGFET includes a lightly doped drain 16 and the second IGFET does not include a lightly doped drain, fig. 5.

But Hung does not disclose the first nitride film does not cover the side surface of the cap film.

However, Kim discloses a semiconductor device in fig. 2H including a lower gate electrode 22a disposed on a gate-insulating layer 21, and an upper gate electrode 29 disposed on the lower gate electrode 22a, an oxide film 24 on the side surface of the lower electrode 22a and a nitride film 25 on a side surface of the upper gate electrode 29, fig. 2H. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of nitride film 25 teaching of Kim with Hung's device, because it would have prevented transformation of the gate electrode as taught by Kim, see abstract.

Regarding claims 18-19, Hung discloses the first and second nitride films have a thickness of less than 6 nm [0020].

But Hung does not disclose the semiconductor is a semiconductor memory device, wherein the first region is a memory cell region a memory cell and the second region is a peripheral circuit region. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the structure teaching of Hung to form the device as claimed, because such memory cell and peripheral region is typical in the art, see Ito 6287907 in fig. 1 (20).

5. Claims 5 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub 2002/0132403 to Hung and US Pub 2002/0001935 to Kim et al. and further in view of US 6448140 to Liaw.

Regarding claim 5, Hung discloses the semiconductor device further including an interlayer insulating film 22 [0022] formed to cover the gate electrode of the IGFET; a contact hole 24, fig. 3c, opened in the interlayer insulating film 22 to expose a source/drain region 15, fig. 3c, of the IGFET; and the source/drain region 16.

But Hung does not disclose the filling the contact hole and electrically connected the S/D region. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to understand that the contact hole 24 of Hung would obviously be filled with conductive material and electrically connected to S/D regions, because such self align contact is typical in the art, see Liaw (6448140) in fig. 7, Uehara (6573132) in fig. 1.

Regarding claim 25, Hung does not disclose the semiconductor device wherein the first lower layer gate electrode 6 has a greater length than the first upper layer gate electrode 6a.

However, Liaw discloses the semiconductor device in fig. 7 wherein the first lower layer gate electrode 3, column 3 line 58, has a greater length than the first upper layer gate electrode 4, column 3 line 60. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the gate length teaching of Liaw with Hung's device because it would have created a thicker sidewall layer and resulting in a smooth, non-protruding sidewall layer as taught by Liaw, column 1 lines 60-67.

6. Claims 21-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pub 2002/0132403 to Hung et al in view of US 6281084 to Akatsu et al.

Regarding claim 21, Hung discloses a semiconductor device in fig. 5, comprising: a first transistor formed in a first region comprising a first upper layer gate electrode 6a formed on and in electrical connection with a corresponding first lower layer gate electrode 6, a first insulating film 10 formed on a majority of a side surface of the first lower layer gate electrode 6, a second insulating film 12 formed on a side surface of the first upper layer gate electrode 6a, the second insulating film 12 having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material, and a first etching stopper film 20 formed on the outside of the first 10 and second insulating films 12, fig. 5, wherein the second insulating film 12 has a film thickness of about 5 nm [0020].

But Hung does not disclose the first etching stop film in contact with a majority of an outside surface of the first insulating film formed on the majority of the side surface of the first lower layer gate electrode.

However, Akatsu discloses a semiconductor device in fig. 2 comprises a lower gate electrode 18 having insulating film 26, and an upper gate electrode 20 having a insulating film 24, fig. 2, the etching stop film 30 in contact with a majority of an outside surface of the insulating film 26 formed on the majority of the side surface of the first lower layer gate electrode 18, fig. 2. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the nitride film 30 teaching of Akatsu with Hung's device, because it would



have improved array gap-fill in the high density dynamic random access memories or embedded memories as taught by Akatsu, column 1 line 5-10.

Regarding claim 22-25, Hung discloses the second insulating film 12 comprises SiN [0021], wherein the first insulating film 10 comprises silicon oxide [0020].

With respect to the 'thermal growth' limitation, it does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

With respect to first lower gate electrode has a greater gate length than the first upper layer gate electrode, Hung and Akatsu discloses the general gate length of the lower and upper electrodes. Accordingly, it would have been obvious to one of ordinary skill in art to use teaching of Hung and Akatsu in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 26, Hung discloses the semiconductor device further including: a second transistor formed in a second region, fig. 5, comprising a second upper layer gate electrode 6a formed on and in electrical connection with a corresponding second lower layer gate electrode 6, a third insulating film 10 formed on a side surface of the second lower layer gate electrode 6 and not on the side surface of the second upper layer gate electrode 6a, a fourth insulating film 12 formed on a side surface of the second upper layer gate electrode 12, the fourth insulating film having a lower thermal growth rate with respect to the second upper layer gate electrode material than the

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thermal growth rate of the third insulating film with respect to the second lower layer gate electrode material, a second etching stopper film 20 formed on the outside of the third and fourth insulating films, fig. 5, a first transistor source/drain region 16 extending laterally below the second etching stopper film 20, fig. 5, and a second transistor source/drain region 18 overlapping a portion of the first transistor source region that does not extend laterally below the second etching stopper film, fig. 5.

With respect to the 'thermal growth' limitation, it does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claim 27, Hung discloses the semiconductor device further including a third transistor source/drain region 16 having a different concentration than either the first or second transistor source/drain regions extending laterally below the first etching stopper film, fig. 5.

### ***Allowable Subject Matter***

7. Claims 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record neither anticipated nor rendered obvious all the limitation of the claim 20 including 20a first contact providing an electrical connection to a first source/drain region of the first IGFET; a second contact providing an electrical connection to a second source/drain region of the second IGFET; and a first spacing from the first contact to the first gate electrode is greater than a second spacing from the second contact to the second gate electrode.

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8. Claims 28 is allowed because the prior art of record neither anticipated nor rendered obvious all the limitation of the claim 28 including a second contact in electrical connection with the first and second S/D region, and isolated from the second lower layer gate electrode by a second insulating thickness that is greater than the first insulating thickness.

### ***Response to Arguments***

9. Applicant's arguments filed on 07 July 2005 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le  
14 July 2005



LONG PHAM  
PRIMARY EXAMINER